Auburn University

Innovation Advancement & Commercialization

Patented Semiconductor Die and Packaging Method

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Reference: Semiconductor Die Attach Method

Lead Inventor

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Reference

Ping Zheng, et al., "Die Attach for High Temperature Electronics Packaging," Proceedings of the International High temperature Electronics Conference, May 13-15, 2008, Albuquerque, NM (Read)

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Overview

Auburn University is seeking licensees for a device and method for attaching semiconductor dies to their chip carriers. The new method relieves the mechanical stress on dies caused by the differences in thermal expansion of the different materials in conventional die attach methods. The new die attach is patterned with voids to allow for the greater thermal expansion in the metal die attach layer while still securely bonding the die to the chip carrier.

Advantages

- Reduces the mechanical stress due to differences in thermal coefficients of expansion through change in die attach geometry rather than composition
- Securely attaches a semiconductor die to its chip carrier
- Reduces cost by eliminating the need to customize alloys to fit thermal properties of the die
- Eliminates problems from changing thermal properties due to interfacial diffusion between the die attach layer and the surface metallization layers

Description

Integrated circuits are formed on semiconductor wafers that are cut into chips otherwise known as dies. The die is bonded to a conductive die attach layer that is then bonded to the chip carrier to form the semiconductor component. This mounting of the die onto the chip carrier through use of a die attach layer directly affects the performance and reliability of the resulting semiconductor component.

Due to the different thermal coefficients of expansion (TCE's) of the die, the die attach layer and the chip carrier, the different rates of thermal expansion can cause mechanical stress on the bonds. This stress can potentially cause cracks or delamination which reduces the reliability of the circuit.

One current solution to the mismatch of TCE's is the formulation of a customized alloy metal to better match the TCE of the die and the chip carrier. However this is not ideal because the TCE's of the die and chip carrier change with temperature in a manner that is specific to each component which makes perfect matching very difficult.

This novel method for attaching the semiconductor dies addresses the TCE problem with a change in geometry rather than metallurgical techniques. The new method involves including a plurality of voids in the die attach layer to allow room for the thermal expansion of the metal. The patterned die attach layer expands into the voids rather than stressing the die. This prevents cracks in the bond seams or delamination. This method is not dependent on the composition of the die attach layer, so interfacial diffusion between the metalized surfaces does not cause a problem at high operating temperatures like is seen in the customized alloy approach.

Licensing Opportunities

- Issued US Patents 7,786,602 and 7,939,376
- These patents are co-owned with The Boeing Company.
- Either or both of these patents are available for immediate non-exclusive licensing through Auburn's customizable "Ready to Sign" licensing program.
- Similar patents are available in the Electronics field.