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Reference: DDS BIST

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Reference

F. Dai, C. Stroud, and D. Yang, "Automatic Linearity and Frequency Response Tests With Built-in Pattern Generator and Analyzer", IEEE Transactions on VLSI Systems, ***14*** *(6), 2006, 561. (Link)*

Status
The invention has been implemented and verified in silicon hardware using field programmable gate arrays.

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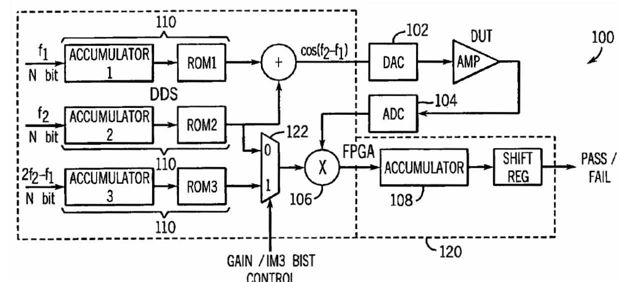
Automatic Analog BIST with Pattern Generator and Analyzer

Overview
Auburn University is seeking licensees for an inexpensive built-in self test (BIST) technique for radio frequency integrated circuits (RFICs). This invention could, for the first time, make complete testing of RFIC chips economically feasible.



A schematic diagram showing a possible implementation of this invention.

Advantages
- Eliminates the need for expensive analog test equipment for RFICs
- Enables complete testing of RFIC chips
- Generates precise frequency tones for analog tests
- Enables accurate phase delay measurement
- Occupies much less area on the chip compared to existing solutions
- Generates more waveforms for tests than competing DDS techniques
- Automatically compensates for temperature, voltage, and other fluctuations due to aging and deterioration of components

Description
The current manual analog testing process for high-speed RFICs is time consuming and costly, rising to as much as 50 percent of the manufacturing cost due to costly test equipment, cumbersome test preparation and the lack of a standardized methodology. As a result, only a small sample of RF circuitry is currently tested.

RFIC testing is sensitive to supply voltage and process variations which makes external testing difficult. Auburn's BIST technique provides analog test capability as well as an efficient technique for calibrating and compensating analog circuitry that is sensitive to temperature, supply voltage and process variations. Existing techniques cannot perform complete tests such as frequency response or noise and modulation, and in some cases require much more chip area overhead than Auburn's method and are not precise enough for analog tests such as analog modulation.

Auburn's invention is a DDS-based BIST approach that generates various modulated waveforms for analog functionality tests. This BIST approach consists of a test pattern generator (TPG) and an output result analyzer (ORA). The TPG can provide precise frequency tones for many analog tests and can implement various waveforms such as chirp, ramp, MSK, QAM and other hybrid modulations. The BIST circuitry has the ability to provide accurate phase information that can be used to tune other functional measurements (such as linearity and gain) for better fault detection. Tests of Auburn's BIST technique show extreme consistency of the output. (In 1000 BIST measurements of an actual ΔP of 14.3dB, BIST output was 14.3 and variance was 0.00003). None of the existing analog testing schemes compare favorably with the comprehensive modulated waveform generation of Auburn's DDS synthesizer (see related Auburn DDS technology), which could make complete testing of RFICs economically feasible.

Licensing Opportunities
- US Patent: 7,428,683
- This patent is available for immediate non-exclusive licensing through Auburn's customizable "Ready to Sign" licensing program.
- Similar patents are available in the Electronics field.